REMARKS

The Office Action dated June 4, 2003, has been received and carefully noted. The above amendments to the specification, and the claims along with the following remarks, are submitted as a full and complete response thereto. As a preliminary matter, Applicants appreciate the indication of allowable subject matter in claims 2, 3, 6, 7,14, and 16-18.

Claims 10, 13, 15, 16, and 19 have been amended, and claim 12 has been cancelled without prejudice. The specification has been amended. Applicants submit that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1-11 and 13-20 are pending in the present application and are respectfully submitted for consideration.

The Office Action objected to claim 10 for being in improper dependent form. Claim 10 is amended to obviate this objection. Accordingly, Applicants request the withdrawal of the objection to claim 10.

The Office Action rejected claims 16-18 under 35 U.S.C. §112, second paragraph, as being indefinite. Claim 16 is amended to more particularly and clearly recite the claimed invention. No new matter is added. The amendment to claim 16 is merely cosmetic in nature and does not affect the scope of the invention. Accordingly, Applicants request the withdrawal of the rejection of claims 16-18 under 35 U.S.C. §112.

The Office Action rejected claims 12, 13, and 19 under 35 U.S.C. §102(e) as being anticipated by Kanazashi et al (U.S. Patent No. 6,337,833, hereinafter "Kanazashi"). The Office Action takes the position that all the features recited in claims 12, 13 and 19 are disclosed in Kanazashi. Claim 12 is cancelled, therefore, the rejection of claim 12 is moot. Applicants submit that claims 13 and 19, by this Amendment, recite subject matter that is neither taught nor suggested by the applied reference.

Claim 13 is directed to a semiconductor integrated circuit comprising a clock buffer, an input buffer, and a clock buffer controller. The clock buffer generates an internal clock signal and the input buffer fetches an input signal in synchronization with the internal clock signal provided from the clock buffer. The clock buffer controller activates the clock buffer, only when there is a change in the input signal, so that the clock buffer generates the

internal clock signal and provides the internal clock signal to the input buffer.

Claim 19 recites a signal fetching method for fetching input signals in synchronization with an internal clock signal generated by a clock buffer in a semiconductor integrated circuit. The method includes the step for activating the clock buffer only when there is a change in the input signal, so that the clock buffer generates the internal clock signal, in synchronization with which the input signals are fetched.

Accordingly, at least one of the essential features of the present invention is a clock buffer controller that activates a clock buffer, only when there is a change in the input signal, so that the clock buffer generates the internal clock signal and provides the internal clock signal to the input buffer. As such, the present invention results in the saving of the power used for generating the internal clock.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the Applicants' invention as set forth in claims 13 and 19, and therefore fails to provide the advantages, which are provided by the present invention.

The present invention recites a clock buffer that generates an internal clock when activated, the input buffer fetches an input signal in synchronization with the internal clock, and the clock buffer controller activates the clock buffer, only when there is a change in the input signal, so that the clock buffer generates the internal clock signal and provides the internal clock signal to the input buffer. As a result, the clock buffer controller detects if there is a change in the input signal. If a change in the input signal is detected then the clock buffer controller activates the clock buffer. When the clock buffer is activated, the internal clock signal is generated and provided to the input buffer for fetching the input signal. In other words, the clock buffer generates the input clock only when necessary so that the power for generating the internal clock can be saved.

Kanazashi is directed to a memory device that includes a data output circuit 40 and is supplied read data from an internal read circuit 30. Kanazashi, however, discloses an internal clock CLK1 for the data output circuit 40, which is supplied to the data output circuit 40 only when the read command is generated. The internal clock CLK3 supplied to input buffers 10 and 14 is not controlled based on the read command. In addition, the clock input buffer 54 for generating the internal clock I-CLK is activated not only when there is a change in the input signal, but also when there is no change in the input signal, as long

as no power down mode PD. In other words, in a period other than the power down mode, the clock input buffer 54 is always activated to generate the internal clock 1-CLK.

Therefore, it is submitted that Kanazashi fails to teach or suggest at least the essential feature of a clock buffer controller that activates the clock buffer, only when there is a change in the input signal, so that the clock buffer generates the internal clock signal and provides the internal clock signal to the input buffer. As a result, Applicants request the withdrawal of the rejection of claims 13 and 19 under 35 U.S.C. 102(e).

Claims 15 and 20 are rejected under 35 U.S.C. §103(a), as being unpatentable over Sakurai (U.S. Patent No. 6,064,627) and Kanazashi et al (U.S. Patent No. 6,337,833). Claims 1, 5, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanazashi and Uchida (U.S. Patent No. 6, 188,641). Claims 4 and 8 are rejected under 35 U.S.C. 103(a) over Kanazashi and Uchida and further in view of Yada et al. (U.S. Patent No. 6,266,294). Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanazashi and Uchida and further in view of Tomita et al (U.S. Patent No. 6,272,069).

It is respectfully submitted that Kanazashi is not prior art under 35 U.S.C. 103(a) via 35 U.S.C. 102(e). The Kanazashi reference is disqualified as prior art against the claimed invention because the subject matter of the reference and the claimed invention were owned by the same person or subject to an assignment to the same person at the time the invention was made. The present application and the Kanazashi reference are assigned to a common owner, Fujitsu Limited. As a result, Kanazashi is not a proper reference under 35 U.S.C. 103(a). Therefore, Applicants request the withdrawal of the rejection of claims 1, 4, 5, 8-11, 15, and 20 under 35 U.S.C. 103(a).

In view of the amendments and the distinctions discussed above, withdrawal of the rejections to claims 1, 4, 5, 8-11, 13, 15, 19 and 20 is respectfully requested. Claims 10, 13, 15, 16, and 19 have been amended, and claim 12 has been cancelled without prejudice. The specification has been amended. No new matter is added. Accordingly, Applicants submit that the application is now in condition for allowance with claims 1-11 and 13-20 contained therein.

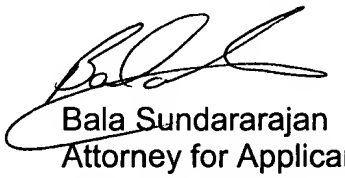
Should the Examiner believe the application is not in condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number

listed below.

In the event this paper is not considered to be timely filed, Applicants respectfully petition for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees, which may be required with respect to this paper to Counsel's Deposit Account 01-2300.

Respectfully submitted,

Arent Fox Kintner Plotkin & Kahn



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Enclosure: